TI Extensa 61X Series
(AcerNote 370P) Notebook

Service Guide

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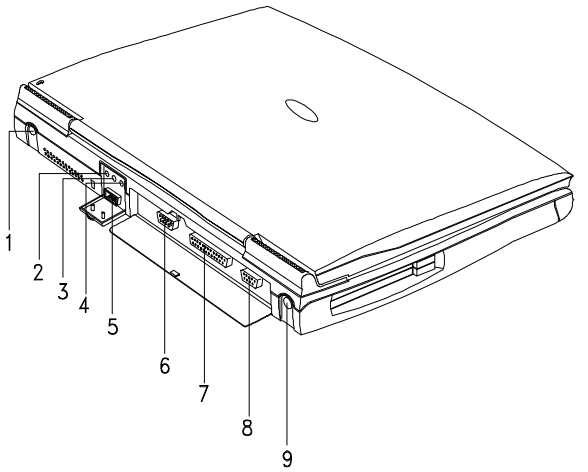
1.1.2 Rear Ports



1 DC-in Port
2 Microphone-in Port
3 Line-in Port
4 Line-out Port
5 External Floppy Drive Connector
6 Serial Port
7 Parallel Port
8 External CRT Port
9 PS/2 Port

Figure 1-2 Rear Ports

The following table describes these ports.

Table 1-1 Port Descriptions

#	Icon	Port	Connects to...
1		DC-in Port	AC adapter and power outlet
2		Microphone-in Port	External 3.5mm minijack condenser microphone
3		Line-in Port	Line-in device (e.g., CD player, stereo walkman)
4		Line-out Port	Line-out device (e.g., speakers, headphones)
5		External Floppy Drive Connector	External floppy drive
6		Serial Port	Serial device (e.g., serial mouse)
7		Parallel Port	Parallel device (e.g., parallel printer)
8		External CRT port	Monitor (up to 1024x768, 256-colors)
9		PS/2 Port	PS/2-compatible device (e.g., PS/2 keyboard, keypad, mouse)

1.1.3 Indicator Light

A two-way indicator light is found on the inside and outside of the display. See figure below.

Table 1-4 CPU Voltage (S1) Settings

CPU Voltage	2.35V	2.45V	2.9V	3.1V
Switch 1	Off	Off	Off	Off
Switch 2	Off	On	Off	Off
Switch 3	On	Off	Off	Off
Switch 4	Off	Off	Off	On

Table 1-5 CPU Speed (SW3) Settings

CPU Speed	120MHz	133MHz	150MHz
Switch 1	Off	On	Off
Switch 2	On	Off	On
Switch 3	Off	Off	On
Switch 4	On	On	On

Table 1-6 Multi-Function Switch (SW2) Settings

Switch		ON	OFF
1	**Keyboard Type (Default OFF)**	-	-
2	**Keyboard Type**	88-key (Japan keyboard)	84/85-key (U.S. keyboard)
3	**Password**	Bypass	Check
4	**Generic boot-up screen show on screen in POST**	No	Yes

1.4.16 Touchpad

Table 1-23 Touchpad Specifications

Item	Specification
Vendor & model name	Synaptics TM1002MPU
Power supply voltage (V)	5 ± 10%
Location	Palm-rest center
Internal & external pointing device work simultaneously	Yes
Support external pointing device hot plug	Yes
X/Y position resolution (points/mm)	20
Interface	PS/2 (compatible with Microsoft mouse driver)

1.4.17 Keyboard

Table 1-24 Keyboard Specifications

Item	Specification
Vendor & model name	SMK KAS1901-0161R (English)
Total number of keypads	84/85 keys
Windows 95 keys	Yes, (Logo key / Application key):
Internal & external keyboard work simultaneously	Yes

1.4.17.1 Windows 95 Keys

The keyboard has two keys that perform Windows 95-specific functions. See Table 1-26.

Table 1-25 Windows 95 Key Descriptions

Key	Description
Windows logo key	Start button. Combinations with this key performs special functions. Below are a few examples: • *Windows* + *Tab* Activate next Taskbar button • *Windows* + *E* Explore My Computer • *Windows* + *F* Find Document • *Windows* + *M* Minimize All • *Shift* + *Windows* + *M* Undo Minimize All • *Windows* + *R* Display Run dialog box
Application key	Opens the application's context menu (same as right-click).

A necessary condition for the notebook to enter hibernation mode is that the reserved space for saving system information on the hard disk must be larger than the combined system and video memory size. Under such conditions, the standby/hibernation hotkey acts as the hibernation hotkey. See the user's manual for information on the Sleep Manager utility.
In this situation, there are four ways to enter hibernation mode:

- Press the standby/hibernation hotkey Fn-F7 (Z^z)

- Set a value for the System Standby/Hibernation Timer in Setup. If the waiting time specified by this time elapses without any system activity, the system goes into hibernation mode

- Enable the Suspend upon Battery-low parameter in Setup. If a battery-low condition takes place, the notebook enters hibernation mode in about five minutes.

- Invoked by the operating system power saving modes

When the notebook enters hibernation mode, the whole system does not consume any power. This is why hibernation mode is also called zero-volt suspend.
To exit hibernation mode, press the power switch (⏻).

When the PCMCIA I/O card is detected, the following warning pop-up message will be displayed on the screen by the BIOS. The system will wait for the specified key to continue.

Warning!!

A PCMCIA card is detected!!

If you are using a fax/modem or LAN cards, please disconnect with server or complete transmission before entering standby/hibernation mode, otherwise :

1) File server will be shut down if LAN card is used.

2) Data will be lost if a modem card is used.

Press <F1> to enter standby/hibernation mode.

Press <F2> to cancel.

2.2.2 Block Diagram

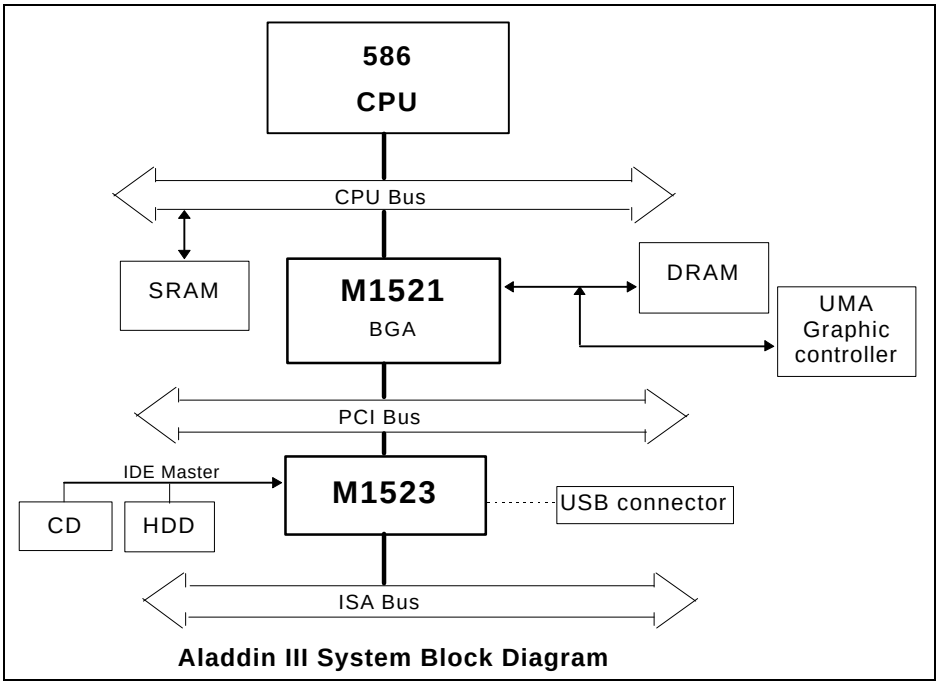


Figure 2-1 Alladin III Block Diagram

2.3 ALI M1523

The M1523 is a bridge between PCI and ISA bus, providing full PCI and ISA compatible functions. The M1523 has Integrated System Peripherals (ISP) on-chip and provides advanced features in the DMA controller. This chip contains the keyboard controller, real-time clock and IDE master controller. This chip also supports the Advanced Programmable Interrupt controller (APIC) interface.

One eight-byte bidirectional line buffer is provided for ISA/DMA master memory read/writes. One 32-bit wide posted-write buffer is provided for PCI memory write cycles to the ISA bus. It also supports a PCI to ISA IRQ routing table and level-to-edge trigger transfer.

The chip has two extra IRQ lines and one programmable chip select for motherboard Plug-and-Play functions. The interrupt lines can be routed to any of the available ISA interrupts.

The on-chip IDE controller supports two IDE connectors for up to four IDE devices providing an interface for IDE hard disks and CD-ROMs. The ATA bus pins are dedicated to improve the performance of IDE master.

The M1523 supports the Super Green feature for Intel and Intel compatible CPUs. It implements programmable hardware events, software event and external switches (for suspend/turbo/ring-in). The M1523 provides CPU clock control (STPCLKJ). The STPCLKJ can be active (low) or inactive (high) in turn by throttling control.

2.3.1 Features

- Technology
  - 0.6µm, triple-metal CMOS process
- Provides a bridge between the PCI bus and ISA bus
  - PCI interface
  - Supports PCI master and slave interface
  - Supports PCI master and slave initiated termination
  - PCI spec. 2.1 compliant (delay transaction support)
- Buffers
  - 8-byte bidirectional line buffers for DMA/ISA memory read/write cycles to PCI bus
  - 32-bit posted-write buffer for PCI memory write and I/O data write (for sound card) to ISA bus
- Provides steerable PCI interrupts for PnP PCI devices
  - Up to eight PCI interrupts routing
  - Level-to-edge trigger transfer
- Enhanced DMA controller
  - Provides seven programmable channels (four for 8-bit data size, three for 16-bit data size)

2.4 ALI M7101 (Power Management Unit)

2.4.1 Features

- Four operating states - ON, DOZE, SLEEP, APM
- Programmable DOZE and SLEEP timer
- Programmable EL timer for backlight control
- Two Programmable APM timers
- Two output pins depending on operating state, each pin is programmable and power configurable
- Provides system activity and EL activity monitorings, includes
  - Video
  - Harddisk
  - Floppy
  - Serial port
  - Parallel port
  - Keyboard
  - Six programmable I/O address groups activity monitor
  - Two programmable memory address groups activity monitor
- Multiple external wake-up events from DOZE or SLEEP to ON states
  - External Push button
  - Cover open
  - Modem Ring
  - RTC alarm
  - DRQ
- Two level battery warning monitors
- 24 General Purpose I/O pins. Each pin can be programmed to become input or output
- 32 External expandable general purpose output signals
- 32 External expandable general purpose input signals
- LCD control
- Rundown monitor detect
- Suspend wake-up detect
- 100-pin PQFP package

Table 2-4 M7101 Pin Descriptions (Continued)

Name	No.	Type	Description
Power Pins			
VDD5 x 3	11,59,76	P	5V VDD input
VDD3 x 2	26,100	P	3.3V VDD input
VDDS x 1	46	P	5V Suspend VDD input. This pin supplies to RI, RTC, HOTKEYJ, COVSW, SUSTATE, PWGD, SUSRSTJ pad.
VSS x 5	1,19,38, 63,90	P	VSS Ground.

2.4.4 Different Pin definition setting

- SLED, CCFT, DISPLAY, SPKCTL, SQWO and GPIOC2 pins are all internal pull high 50K ohms. The blank part of following table means keeping the original pin definition.
- When SLED default is pulled high, the chip will be in normal mode.
- When SLED is pulled low by 4.7K resistor, the chip will be in test mode.
- When GPIOC2 pull low, the PCI ports are 0078/007A and offset 0F6h D15 will be set, otherwise, 0178/017A.

Table 2-5 M7101 Different Pin Definition Setting

Original pin definition	CCFT pull low 4.7K	DISPLAY pull low 4.7K	SPKCTL pull low 4.7K	SQWO pull low 4.7K
	offset 0F6h D1=1	offset 0F6h D2=1	offset 0F6h D3=1	offset 0F6h D4=1
GPIOA5				GPIOWB
GPIOA4				GPIORBJ
GPIOA1			GPIOWA	
GPIOA0			GPIORAJ	
GPIOB7		STPCLKJ		
GPIOB6		AMSTATJ		
GPIOB5		OUT_INIT		
GPIOB4		OUT_INTR		
GPIOB3		IN_BRDYJ		
GPIOB2		IN_INIT		
GPIOB1		IN_SMIJ		
GPIOB0		IN_INTR		
GPIOC2	BIOSA17			
GPIOC1	BIOSA16			
GPIOC0	ISA16			

Table 2-10 C&T 65550 Pin Descriptions (continued)

Pin#	Pin Name	Type	Description
CPU Direct / VL-Bus Interface (continued)			
43	BE0# (BLE#)	In	Byte Enable 0. Indicates data transfer on D7:D0 for the current cycle.
32	BE1#	In	Byte Enable 1. Indicates data transfer on D15:D8 for the current cycle.
21	BE2#	In	Byte Enable 2. Indicates data transfer on D23:D16 for the current cycle.
10	BE3#	In	Byte Enable 3. BE3# indicates that data will transfer over the data bus on D31 :24 during the current access.
179 180 182 183 185 186 187 188 189 190 191 192 193 194 195 196 197 189 199 200 201 28 29 30 53 54	A2 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12 A13 A14 A15 A16 A17 A18 A19 A20 A21 A22 A23 A24 A25 A26 A27	In In In In In In In In In In In In In In In In In In In In In In In In In In	System Address Bus. In VL-Bus, and direct CPU interfaces, the address pins are connected directly to the bus. In internal clock synthesizer test mode (TS# = 0 at Reset), A24 becomes VCLK out and A25 becomes MCLK out. A26 and A27 may be alternately used as General Purpose I/O pins or as Activity Indicator and Enable Backlight respectively (see panel interface pin descriptions, and FROF and FROC for more details). If A26 and A27, are used as GPIO pins, they may be programmed as a 2-pin CRT Monitor DDC interface (VESA™ "Display Data Channel" also referred to as the "Monitor Plug-n-Play" interface). Either A26 or A27 may also be used to output, Composite Sync for support of an external NTSC / PAL encoder chip.

Table 2-10 C&T 65550 Pin Descriptions (continued)

Pin#	Pin Name	Type	Description
Power / Ground and Standby Control (continued)			
66 63 89	DCC DGND DGND	VCC GND GND	Power / Ground (Bus Interface) 5V±10% or 3.3V±0.3V.
158 161 142 139 108 105	MVCCA MGNDA MVCCB MGNDB MVCCC MGNDC		Power / Ground (Bus Interface) 5V±10% or 3.3V±0.3V.

FLAT PANEL DISPLAY INTERFACE (CONFIGURATION BY PANEL TYPES)

Table 2-11 Flat Panel Display Interface Configurations

65550		Mono SS	Mono DD	Mono DD	Color TFT	Color TFT	Color TFT HR	Color STN STN SS	Color STN SS	Color STN DD	Color STN DD	Color STN DD
Pin#	Pin Name	8-bit	8-bit	16-bit	9/12/16 bit	18/24 bit	18/24 bit	8-bit (X4bP)	16-bit (4bP)	8-bit (4bP)	16-bit (4bP)	24 bit
71	P0	-	UD3	UD7	B0	B0	B00	R1	R1	UR1	UR0	UR0
72	P1	-	UD2	UD6	B1	B1	B01	B1	G1	UG1	UG0	UG0
73	P2	-	UD1	UD5	B2	B2	B02	G2	B1	UB1	UB0	UB0
74	P3	-	UD0	UD4	B3	B3	B03	R3	R2	UR2	UR1	LR0
75	P4	-	LD3	UD3	B4	B4	B10	B3	G2	LR1	LR0	LG0
76	P5	-	LD2	UD2	G0	B5	B11	G4	B2	LG1	LG0	LB0
78	P6	-	LD1	UD1	G1	B6	B12	R5	R3	LB1	LB0	UR1
79	P7	-	LD0	UD0	G2	B7	B13	B5	G3	LR2	LR1	UG1
81	P8	P0	-	LD7	G3	G0	G00	SHFCLKU	B3	-	UG1	UB1
82	P9	P1	-	LD6	G4	G1	G01	-	R4	-	UB1	LR1
83	P10	P2	-	LD5	G5	G2	G02	-	G4	-	UR2	LG1
84	P11	P3	-	LD4	R0	G3	G03	-	B4	-	UG2	LB1
85	P12	P4	-	LD3	R1	G4	G10	-	R5	-	LG1	UR2
86	P13	P5	-	LD2	R2	G5	G11	-	G5	-	LB1	UG2
87	P14	P6	-	LD1	R3	G6	G12	-	B5	-	LR2	UB2
88	P15	P7	-	LD0	R4	G7	G13	-	R6	-	LG2	LR2
90	P16	-	-	-	-	R0	R00	-	-	-	-	LG2
91	P17	-	-	-	-	R1	R01	-	-	-	-	LB2
92	P18	-	-	-	-	R2	R02	-	-	-	-	UR3
93	P19	-	-	-	-	R3	R03	-	-	-	-	UG3
94	P20	-	-	-	-	R4	R10	-	-	-	-	UB3
95	P21	-	-	-	-	R5	R11	-	-	-	-	LR3
96	P22	-	-	-	-	R6	R12	-	-	-	-	LG3
97	P23	-	-	-	-	R7	R13	-	-	-	-	LB3
70	SHFCLK	SHFCLK	SHFCLK	SHFCLK	SHFCLK	SHFCLK	SHFCLK	SHFCLK	SHFCLK	SHFCLK	SHFCLK	SHFCLK
	Pixels / Clock:	8	8	16	1	1	2	2-2/3	5-1/3	2-2/3	5-1/3	8

Table 2-13 PCI1131 Pin Descriptions (Continued)

TERMINAL NAME NO.	I/O TYPE	FUNCTION
PCI Address and Data Terminals		
C/BE3 180 C/BE2 192 C/BE1 203 C/BE0 5	I/O	8us commands and byte enables. These are muitiplexed on the same PCI terminals. During the address phase, C/BE-0 define the bus command. During the data phase, C /ENEW-O are used as byte enables. The byte enables determine which byte lanes carry meaningful data. C/BE0 applies to byte 0 (AD7-0), C/BE1 applies to byte 1 (AD15-8), C/BE2 applies to byte 2 (AD23-16),and C/BE3 applies to byte 3 (AD31-24).
PAR 202	I/O	Parity. As a PCI target during PCI read cycles, or as PCI bus master during PCI write cycles, the PCI 1131 calculates even parity across the AD and C/BE buses and outputs the results on PAR, delayed by one clock.
PCI Interface Control Terminals		
DEVSEL 197	I/O	Device select. As a PCI target, the PCI1131 asserts DEVSEL to claim the current cycle. As a PCI master, the PCI1131 monitors this signal until a target responds or a time out occurs.
FFAME 193		Cycle frame. Driven by the current master to indicate the beginning and duration of an access, FRAME I/O is low (asserted) to indicate that a bus transaction is beginning. While FFGI9IE is asserted, data transfers continue. When FRAME is sampled high (deasserted), the transaction is in the final data phase .
GNT 168	I	Grant. Driven by the PCI arbiter to grant the PCI1131 access to the PCI bus after the current data transaction has completed.
IDSEL 182	I	Initialization device select. IDSEL selects the PCI1t31 during configuration accesses. IDSEL can be connected to one of the upper 24 PCI address lines.
IRDY 195	I/O	Initiator ready. IRDY indicates the bus master's ability to complete the current data phase of the transaction. IRDY is used in conjunction with IRDY. A data phase is completed on any clock where I/O both IRDY and TRDY are sampled low (asserted). During a write, IRDY indicates that valid data is present on AD31-0. During a read, IRDY indicates that the master is prepared to accept data. Wait cycles are inserted until both IRDY and TRDY are low (asserted) at the same time. This signal is an output when the PCI1131 is the PCI bos master and an input when the PCI bus target.
STOP 198	I/O	Stop. This signal is driven by the current PCI target to request the master to stop the current transaction.
PERR 99	I/O	Parity error. This signal is driven by the PCI target during a write to indicate that a data parity error has . been detected.
REQ 169	O	Request. Asserted by the PCI1131 to request access to the PCI bus as a master.
SERR 200	O	O System error. Output pulsed from the PCI1131 indicating an address parity error has occurred.

Table 2-13 PCI1131 Pin Descriptions (Continued)

TERMINAL NAME	NO	I /O TYPE	FUNCTION
Interrupt Terminals			
IRQ15/ RI_OUT	163	I/O	Interrupt Request 15. This terminal indicates an interrupt request from one of the PC Cards. RI_OUT allows the RI input from the 1 6-bit PC Card, CSTSCHG from CardBus Cards or PC Card removal events to be output to the system. This signal is configured in the Card Control Register of the TI Extension Registers.
PC Card Power Switch Terminals			
LATCH	150	O	Power Switch Latch is asserted by the PCI1131 to indicate to the PC Card power switch that the data on the DATA line is valid.
CLOCK	151	O	Power Switch Clock. Information on the DATA line is sampled at the rising edge of CLOCK. The frequency of the clock is derived from dividing the PCICLK by 36. The maximum frequency of this signal is 2 MHz.
DATA	152	O	Power Switch Data is used by the PCI1131 to serially communicate socket power control information.
Speaker Control Terminal			
SPKROUT/ SUSPEND	149	I/O	Speaker. SPKROUT carries the digital audio signal from the PC Card. SUSPEND, when enabled, this signal places the PCI1131 in PCI1131 Suspend Mode (Section 6.0) . This pin is configured in the Card Control Register (Section 7.29) of the TI Extension Registers.
Power Supply Terminals			
GND	13,22,44 75 96,129, 153, 167, 81 194,207	I	Device ground terminals
VccA	120	I	Power-supply terminal for PC Card A (5V or 3.3V)
VccB	38	I	Power-supply terminal for PC Card B (5V or 3.3 V)
VccP	148, 172	I	Power-supply terminal for PCI interface (5V or 3.3V)
Vcc	7, 31, 64, 86, 113, 143,164, 175, 187, 201	I	Power-Supply terminal for core logic (3.3V)

Table 2-14 NS87336VJG Pin Descriptions (continued)

Pin	No.	I/O	Description
/MSEN0 /MSEN1 (Normal Mode)	50, 49	I	Media Sense. These pins are Media Sense input pins when bit 0 of FCR is 0. Each pin has a 10 KΩ internal pull-up resistor. When bit 0 of FCR is 1, these pins are Data Rate output pins and the pull-up resistors are disabled.
/MSEN0 /MSEN1 (PPM Mode)	86, 84	I	Media Sense. These pins gives additional Media Sense signals for PPM Mode and PNF = 0.
/MTR0 /MTR1 (Normal Mode)	44, 41	O	FDC Motor Select 0, 1. These are the motor enable lines for drives 0 and 1, and are controlled by bits D7-D4 of the Digital Output register. They are active low outputs. They are encoded with information to control four FDDs when bit 4 of the Function Enable Register (FER) is set. MTR0 exchanges logical motor values with MTR1 when bit 4 of FCR is set.
/MTR1 (PMM Mode)	82	O	FDC Motor Select 1. This pin offers an additional Motor Select 1 signal in PPM mode when PNF = 0. This pin is the motor enable line for drive 1 when bit 4 of FCR is 0. It is the motor enable line for drive 0 when bit 4 of FCR 1. This signal is active low
PD	43	O	FDC Power Down. This pin is PD output when bit 4 of PMC is 1. It is /DR1 when bit 4 of PMC is 0. PD is active high whenever the FDC is in power-down state, either via bit 6 of the DSR (or bit 3 of FER, or bit 0 of PTR), or via the mode command.
PD0-7	92-89, 87-84	I/O	Parallel Port Data. These bidirectional pins transfer data to and from the peripheral data bus and the parallel port Data Register. These pins have high current drive capability.
PE	81	I	Parallel Port Paper End. This input is set high by the printer when it is out of paper. This pin has a nominal 25 KΩ pull-down resistor attached to it.
PNF	47	I	Printer Not Floppy. PNF is the Printer Not Floppy pin when bit 2 of FCR is 1. It selects the device which is connected to the PPM pins. A parallel printer is connected when PNF = 1 and a floppy disk drive is connected when PNF = 0. This pin is the DRV2 input pin when bit 2 of FCR is 0.
/RD	17	I	Read. Active low input to signal a data read by the microprocessor.
/RDATA (Normal Mode)	33	I	FDD Read Data. This input is the raw serial data read from the floppy disk drive.
/RDATA (PPM Mode)	89	I	FDD Read Data. This pin supports an additional Read Data signal in PPM Mode when PNF = 0.

Table 2-17 T62.062.C Electrical Characteristics Table (Continued)

Parameter	Symbol	Condition	MIN	TYP	MAX	UNITS
SAFETY OPERATION						
Over voltage protect by Software		NiMH LiB_Ion		16.2 13		V V
Note 1: External Adapter: Voltage limit 20V1V with maximum 24V over voltage as well as over current protection.						

2.9.5 Pin Diagram

DC_BAT_OUT	1 o	o 2	DC_BAT_OUT
DC_BAT_OUT	3 o	o 4	DC_BAT_OUT
GND	5 o	o 6	GND
PERIPHERAL SYSTEM ON	7 o	o 8	5VSB_OUT
SYSTEM ON	9 o	o 10	DISABLE
BT_QCHG	11 o	o 12	AD5V
SMI	13 o	o 14	S.I.U.
TH	15 o	o 16	BL1#
ID	17 o	o18	BL2#
GND	19 o	o20	BAT_IN_USE#
BT_VS	21 o	o22	GND
BT+	23 o	o24	BT+
BT+	25 o	o26	BT+

Figure 2-18 T62.062.C Pin Diagram

2.11.3 Top Overlay

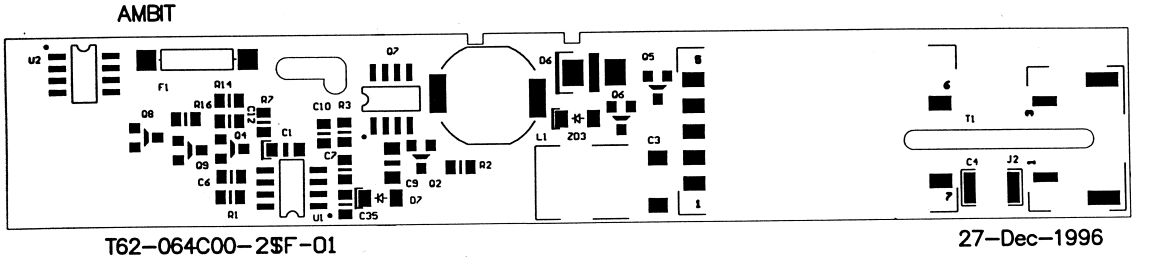


Figure 2-20 T62.064.C DC-AC Inverter Top Overlay diagram

2.11.4 Bottom Overlay

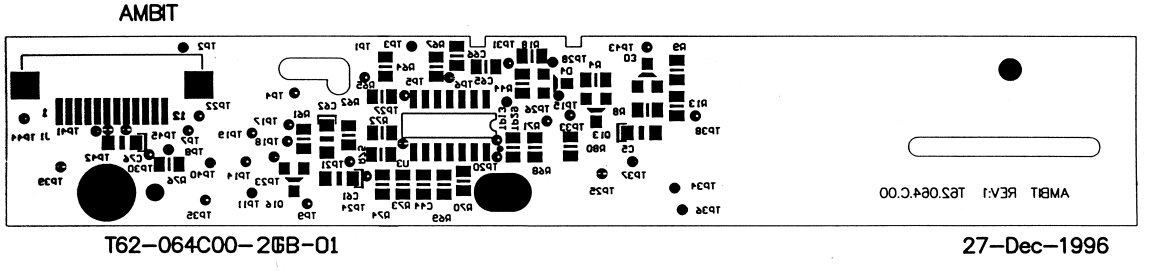


Figure 2-21 T62.064.C DC-AC Inverter Bottom Overlay diagram

3.4.3 System Boot Drive Control

This parameter determines which drive the notebook boots from when you turn it on. The following table lists the three possible settings.

Table 3-4 System Boot Drive Control Settings

Setting	Description
Drive A Then C (default)	Notebook boots from floppy drive A. If there is no system disk in drive A, the notebook boots from hard disk C. If the hard disk is a non-system disk, an error message appears.
Drive C Then A	Notebook boots from hard disk C. If hard disk C is not a system disk, the notebook boots from floppy drive A. If no diskette is present or if the diskette in floppy drive A is a non-system disk, an error message appears.
Drive C	Notebook boots from hard disk C. If hard disk C is not a system disk, an error message appears.
Drive A	Notebook boots from floppy drive A. If no diskette is present or if the diskette in floppy drive A is a non-system disk, an error message appears.

An installed PCMCIA bootable card overrides the System Boot Drive setting. The notebook supports SRAM card boot.

3.4.4 CD-ROM Bootable

When enabled the notebook checks the CD-ROM drive first and boots from there, if possible, before checking the System Boot Drive control setting.

There are two image types/formats for CD-ROMs - floppy drive and hard disk. See Table 3-5 for a description.

Table 3-5 CD-ROM Image Descriptions

Image Type	Upon Boot-up…
Floppy Drive	CD-ROM drive becomes drive A and the floppy drive becomes drive B. The hard disk drive remains drive C.
Hard Disk	CD-ROM drive becomes drive C and the hard disk drive becomes drive D. The floppy drive remains drive A.

Disassembly and Unit Replacement

This chapter contains step-by-step procedures on how to disassemble the notebook computer for maintenance and troubleshooting.

To disassemble the computer, you need the following tools:

- Wrist grounding strap and conductive mat for preventing electrostatic discharge
- Flat-bladed screwdriver
- Phillips screwdriver
- Hexagonal screwdriver
- Tweezers
- Plastic stick

The screws for the different components vary in size. During the disassembly process, group the screws with the corresponding components to avoid mismatch when putting back the components.

4.5.2 Removing the Internal Drive

1. Pull up and remove the FDD/CD module latches.
2. Unplug the internal drive cable (CN14/CN17 for CD-ROM or CN14 for FDD).
3. Pull out the internal drive and set it aside.

Ensure the drive cables do not become hooked on the inside frame assembly when removing and reinstalling the drive.

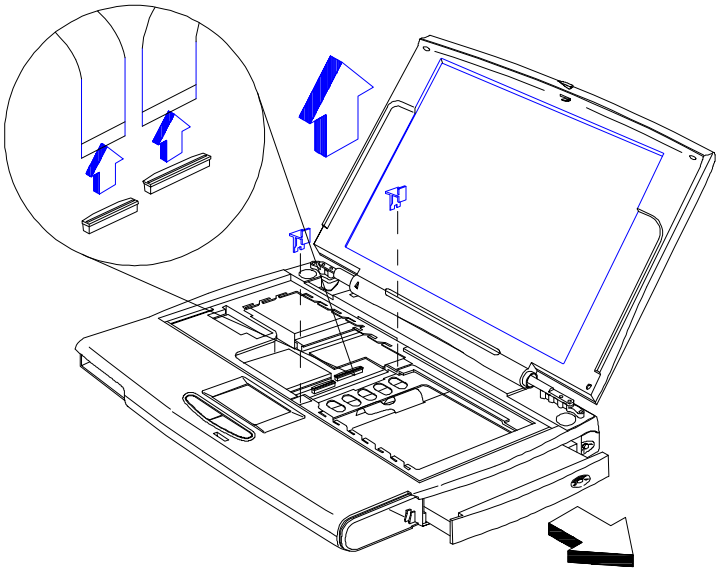


Figure 4-11 Removing the Internal Drive

4.5.9 Removing the Touchpad

The touchpad is connected to the top cover. Follow these steps to remove the touchpad assembly:

1. Peel off the mylar.
2. Remove the three screws and disconnect the touchpad cable (J2), then remove the touchpad main sensor and connector unit.
3. Lift up and remove the touchpad.
4. Lift up and remove the touchpad buttons.

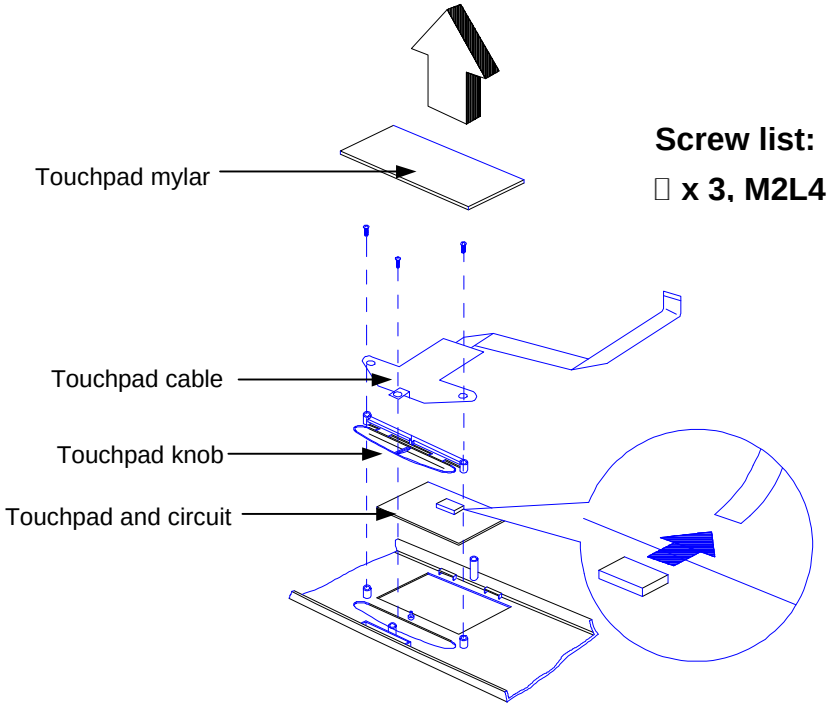


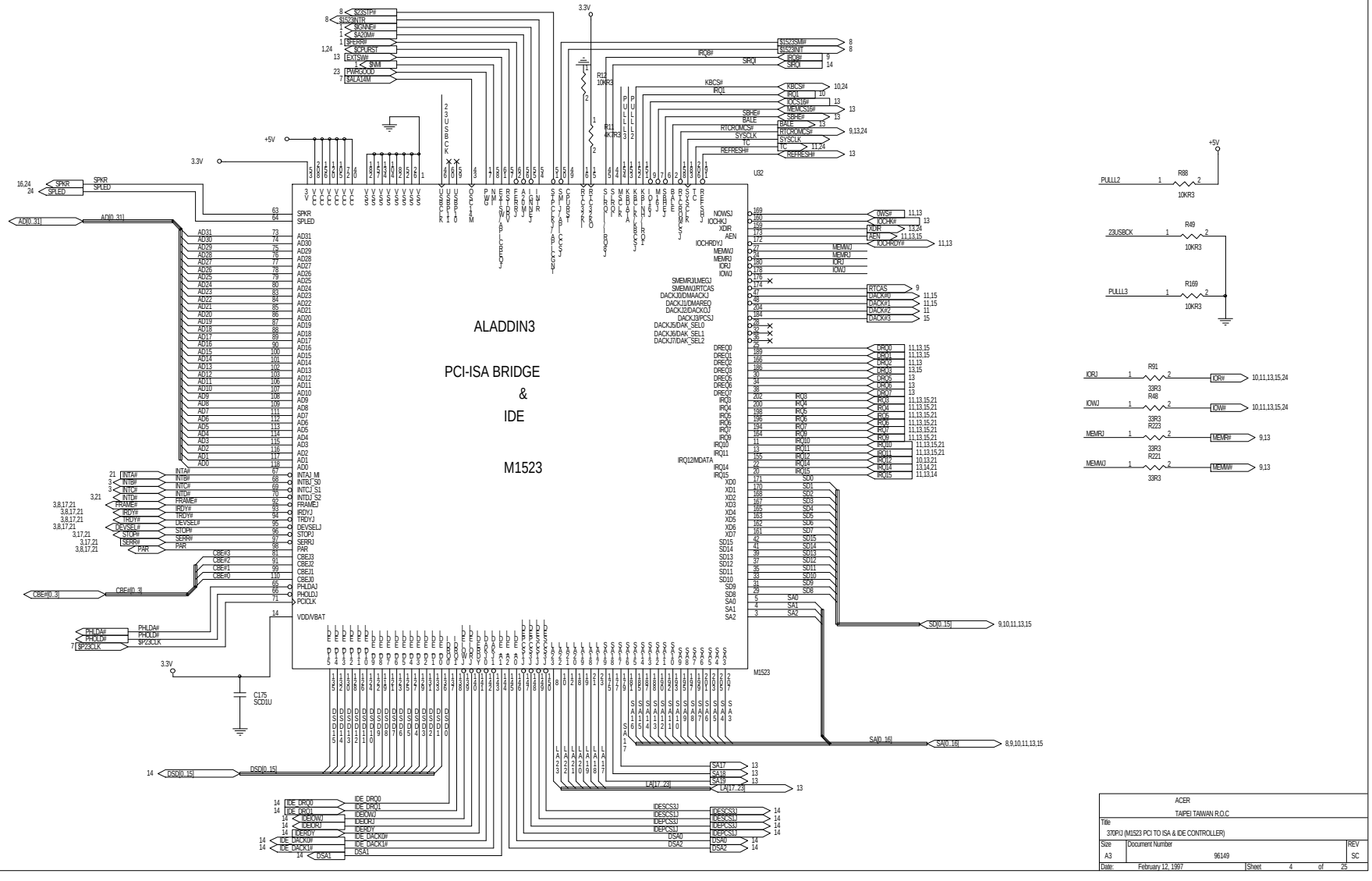
Figure 4-26 Removing the Touchpad

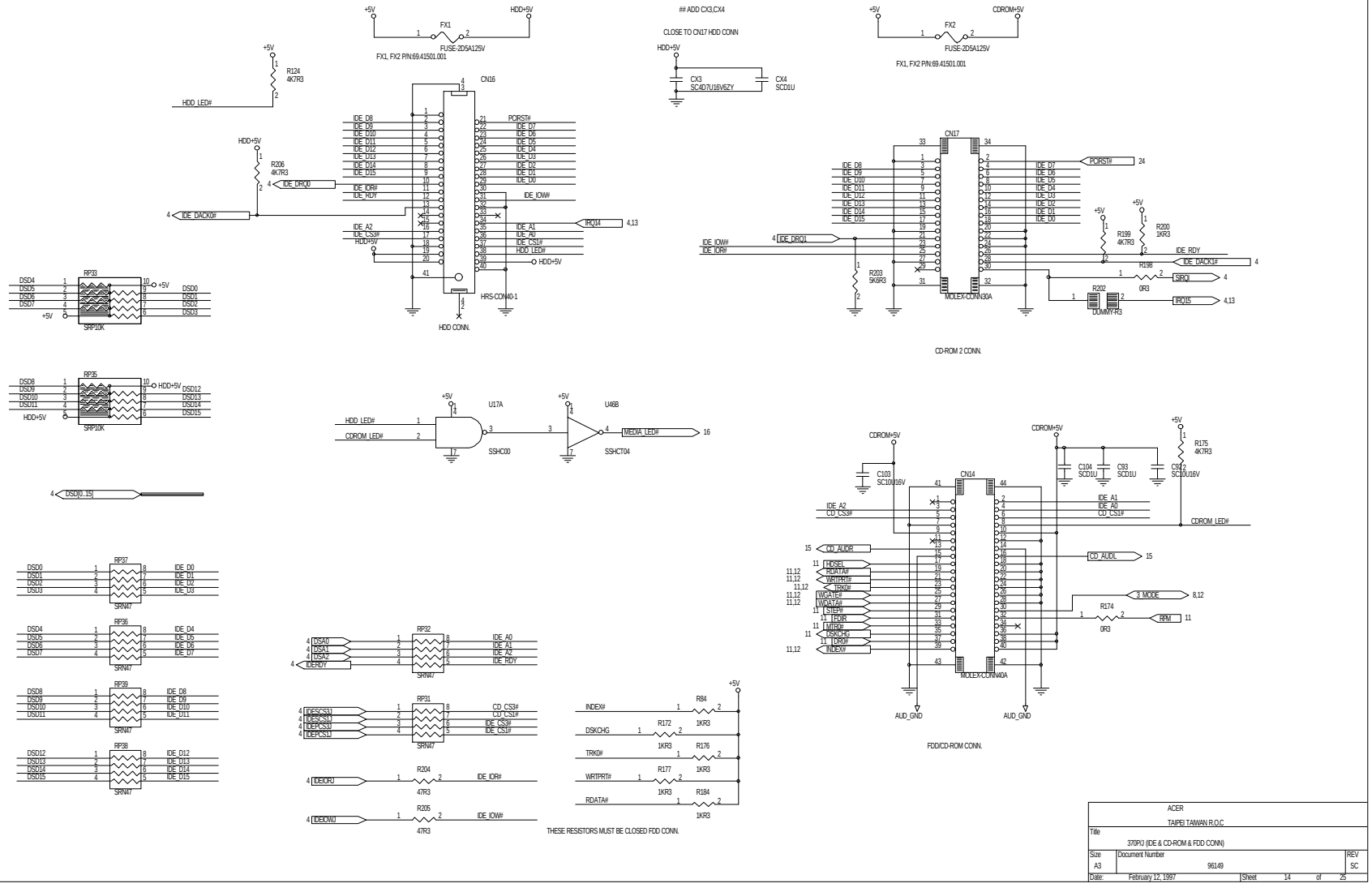
Spare Parts

This appendix lists the spare parts of the notebook TI EXTENSA 610.

Table C-1 Spare Parts List

	PART NAME	ACER P/N	TI P/N	Ref. Exploded View	COMMENTS
<< MECHANICAL & MODULES >>					
1	IC CHARGE (power supply charger bd)	05.62062.020	9811768-0001	56	
2	FAN 5V UDQFC3E09 105MM	23.10029.011	9811769-0001	32	
3	ADT (AC Adapter w/o power cord)	25.10052.001	9811770-0001		see options for AC adapter with cord
4	HEAT SINK-U(2) AL AN370	34.46925.001	981177100001	30	
5	CASE UPPER (TOP) 370P/TI	39.46901.031	9811772-0001	21	w/o label
6	C.A FPC TOUCH PAD 370P	6M.48415.001	9811774-0001	24, 25	w/cable, bracket
7	C.A FPC AUDIO BD 370P	50.48402.001	9811775-0001		
8	HDD 1083MB TOSHIBA/MK1002MAV	56.02775.001	9811776-0001		without case or cable
9	HDD 1440MB HIT-DK225A-14	56.02568.031	9815585-0001		
10	HDD 2160MB IBM/DTNA -22160	56.02941.011	9815586-0001		
11	HDD TRANSFER BD	55.48403.001	9811802-0001		w/ connector
12	ASSY HDD UPPER COVER	60.48412.101	9811783-0001	44	w/mylar
13	ASSY HDD LOWER COVER	60.48418.101	9811785-0001	46	w/mylar, belt sponge
14	TOUCHPAD SYNAP/TM1202MPU-156-1	56.17450.011	9811777-0001	22	w/o label
15	ASSY HINGE (COVER) CAP(R) 050 AN370	60.46906.001	9811778-0001	7	w/net speaker, hinge cap
16	ASSY HINGE (COVER) CAP(L) 050 AN370	60.46906.011	9811779-0001	10	w/net speaker, hinge cap
17	ASSY LOWER CASE (BASE) 370P	60.48411.001	9811782-0001		w/bracket, pcmcia cover, I/o door, knob power, foot rub, cover ext FDD, simm cover
18	ASSY CHASSIS AN370P	60.48413.001	9811784-0001		w/speaker, battery bd, PCMCIA door, mylar, cover switch
19	FDD EXTERNAL 370	91.46905.012	9811788-0001		w/cable
20	ASSY CD-ROM KIT (V32)	91.46928.023	9811789-0001		w/bracket, cable, bezel, knob
21	C.A. ASSY CD-FPC,EXT 61X	50.46903.002	9815582-0001	58	
22	CD-ROM BEZEL	41.46903.001	9815587-0001		


ALADDIN3
PCI-ISA BRIDGE
&
IDE
M1523
U82
M1523
+5V
3.3V
SPKR
SPLED
AD[0..31]
CBE#[0..3]
PHLDA#
PHOLD#
SP23CLK
C175
SCD1U
DSD[0..15]
SA[0..16]
SD[0..15]
LA[17..23]
SA17
SA18
SA19
IDE_DRQ0
IDE_DRQ1
IDEIOWJ
IDEIORJ
IDERDY
IDE_DACK0#
IDE_DACK1#
DSA1
IDESCS3J
IDESCS1J
IDEPCS3J
IDEPCS1J
DSA0
DSA2
PULL2
PULL3
23USBCK
R88
R49
R169
10KR3
R91
33R3
R48
R223
R221
IORJ
IOWJ
MEMRJ
MEMWJ
IOR#
IOW#
MEMR#
MEMW#
ACER
TAIPEI TAIWAN R.O.C
Title
370PIJ (M1523 PCI TO ISA & IDE CONTROLLER)
Size
A3
Document Number
96149
REV
SC
Date:
February 12, 1997
Sheet
4
of
25


FX1
FUSE-2D5A125V
FX1, FX2 P/N:69.41501.001
HDD+5V
+5V
R124
4K7R3
HDD_LED#
CN16
R206
4K7R3
IDE_DRQ0
IDE_IOR#
IDE_RDY
IDE_DACK0#
IDE_IOW#
IRQ14
4,13
IDE_A2
IDE_CS3#
HDD+5V
HRS-CON40-1
HDD CONN.
ADD CX3,CX4
CLOSE TO CN17 HDD CONN
CX3
SC4D7U16V6ZY
CX4
SCD1U
FX2
FUSE-2D5A125V
FX1, FX2 P/N:69.41501.001
CDROM+5V
CN17
IDE_DRQ1
R203
5K6R3
R199
4K7R3
R200
1KR3
R198
0R3
R202
DUMMY-R3
MOLEX-CON30A
CD-ROM 2 CONN.
RP33
SRP10K
RP35
SRP10K
U17A
SSHC00
U46B
SSHCT04
HDD_LED#
CDROM_LED#
MEDIA_LED#
16
DSD[0..15]
RP37
RP36
RP39
RP38
SRN47
RP32
RP31
IDECS3J
IDECS1J
IDECS3J
IDECS1J
IDEIORJ
IDEIOWJ
R204
R205
47R3
THESE RESISTORS MUST BE CLOSED FDD CONN.
C103
SC100U16V
C104
SCD1U
C93
SCD1U
C92
SC10U16V
R175
4K7R3
CN14
CD_AUDR
CD_AUDL
HDSEL
RDATA#
WRTPRT#
TRK0#
WGATE#
WDATA#
STEP#
TFDIR
MTR0#
DSKCHG
DRS0#
INDEX#
3_MODE
R174
0R3
RRM
MOLEX-CON40A
AUD_GND
FDD/CD-ROM CONN.
R84
R172
R176
R177
R184
1KR3
ACER
TAIPEI TAIWAN R.O.C.
Title
370PJ (IDE & CD-ROM & FDD CONN)
Size
A3
Document Number
96149
REV
SC
Date:
February 12, 1997
Sheet
14
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25